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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/847,032	04/30/2001	Lester S. Sanders	X-858 US	5645

24309 7590 04/21/2004

XILINX, INC
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EXAMINER	
PHAN, THAI Q	

ART UNIT	PAPER NUMBER
2128	9

DATE MAILED: 04/21/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/847,032	Applicant(s) SANDERS, LESTER S.	
	Examiner Thai Phan	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *30 April 2001*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-21* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-21* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 April 2001* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

This Office Action is in response to patent application S/N: 09/847,032, filed on 04/30/2001. Claims 1-21 are pending in the action.

Drawings

The drawings filed on 04/30/2001 are acceptable for examination.

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 1-21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Jain, Prem, US patent no. 6,044,211.

As per claim 1, Jain discloses a method and system for circuit design and synthesis with feature limitations very similar to the claimed invention. According to Jain, the design method includes steps of

Receiving a first low level design or design representation for a target circuit (Figs. 4 and 5, col. 9, line 48 to col. 12, col. 16, lines 28-60,for example),

Transforming the first low level design representation into a synthesizable or simulatable high level representation (col. 19, line 44 to col. 22),

And processing the high level design representation to generate a low-level design representation for a target circuit dependent on technology or silicon. Jain does not expressly disclose compilation for targeting a second integrated circuit as claimed.

Practitioner in the art at the time of the invention was made would have found Jain disclosure of target compilation for a specific technology and silicon process in col. 15, line 44 to col. 16, line 27, col. 23, lines 35 to 55, for example would imply the claimed limitation of compilation for a second target circuit representation because the process for compilation for a specific technology or silicon above results in a circuit representation which depends and differs from the first representation. In other words, it would be a second target circuit representation.

As per claims 2-5, Jain discloses the claimed limitations such as logic devices, gate arrays, programmable logic devices, etc which are called digital devices.

As per claims 6-9, Jain discloses a plurality of programming languages would be used in ASIC design environment. Such languages would include HDL, VHDL, RTL, etc. to express logic operations or functions. Thus, the design language would include other well known languages such as ABEL code as claimed.

As per claim 10, Jain discloses compiling object codes representation for circuit design such that the compiled codes would be simulated (simulatable codes) (col. 19, line 55 to col. 21, line 13, cols. 23-24, for example).

As per claims 11-21, Jain discloses various digital devices being designed and synthesized as claimed. Jain also discloses design languages used in the design

would include HDL, VHDL, RTL, Verilog, C, etc. This would include other design languages known in the art of digital design such as the claimed ABEL codes.

Conclusion

The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

1. US patent no. 5,452,227, issued to Kelsey et al., on Sept. 1995
2. US patent no. 6,086,625, issued to Shouen, Akihisa, on July 2000
3. US patent no. 6,216,259 B1, issued to Guccione et al, on Apr. 2001
4. US patent no. 6,493,648 B1, issued to Anderson, Glen, on Dec. 2002
5. US patent application no. US 2003/0216901 A1, issued to Schaumont et al, on Nov. 2003.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to paten examiner Thai Phan whose telephone number is 703-305-3812.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kevin Teska can be reached on 703-305-9704. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Thai Phan
Apr. 18, 2004

Thai Phan
Thai Phan
Patent Examiner
AU: 2128